A Highly Tunable ASIC Prototype for Reading Out Scintillators and Providing Real-Time Pulse Shape Discrimination

Jyothisraj Johnson[1], Billy Boxer[1], Carl Grace[2], Mani Tripathi[1]

[1]University of California, Davis, Department of Physics, Davis, CA 95616, USA

[2]Lawrence Berkeley National Laboratory, Engineering Division, Berkeley, CA 94720, USA

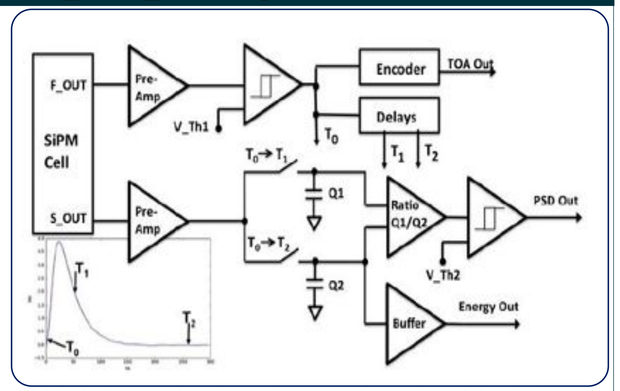
Nuclear Science & Security Consortium

Key ASIC Prototype Design Goals

- Develop an application specific integrated circuit (ASIC) to serve as a front-end system for read-out of plastic/organic scintillator materials when coupled to SiPMs, while providing real-time pulse shape discrimination (PSD)
  - Demonstrate key electronics needed for a portable and compact pixelated neutron camera
- Ensure maximum programmability/tunability of all parts of chip design for a first prototype and that all important nodes are available as external outputs
- Real-time fast neutron/gamma PSD is implemented through an analog version of a ratio partial/total integration of incident waveform
- The ASIC contains a synthesized digital core that allows for high tunability and programmability of various parts of the parallel integration setup. This allows for use with various plastic/organic scintillator materials
  - The ASIC front-end system is now designed for variable gain and dual-polarity input capability

Summary of PSD_CHIP_v2 Design

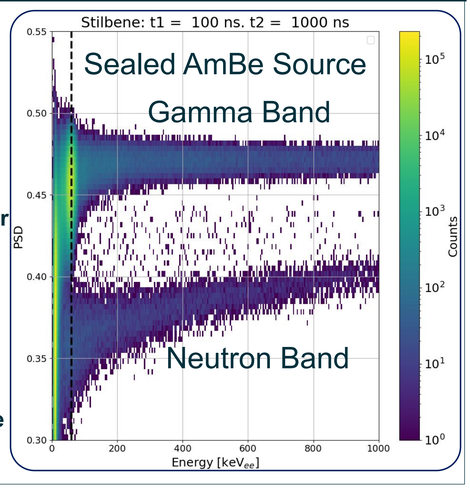
- The second prototype ASIC we have developed, PSD_CHIP_v2 is a 4CH design
- The chip is designed to read out SensL's line of SiPM arrays, with each SiPM containing two outputs: a fast capacitively coupled output (FOUT) and a standard resistively coupled output (SOUT). The former is used for triggering and the latter is the input to the real-time PSD circuitry
- Adjustable gain in the front-end stage can be set from a transimpedance gain of ~30x to ~180x
- The chip's front-end consists of a NMOS+PMOS regulated common gate (RCG) amplifier that can either sink or source current depending on polarity of input current pulse from the SiPM cell



A block diagram that shows the general overview of the single channel signal processing stages is shown above.

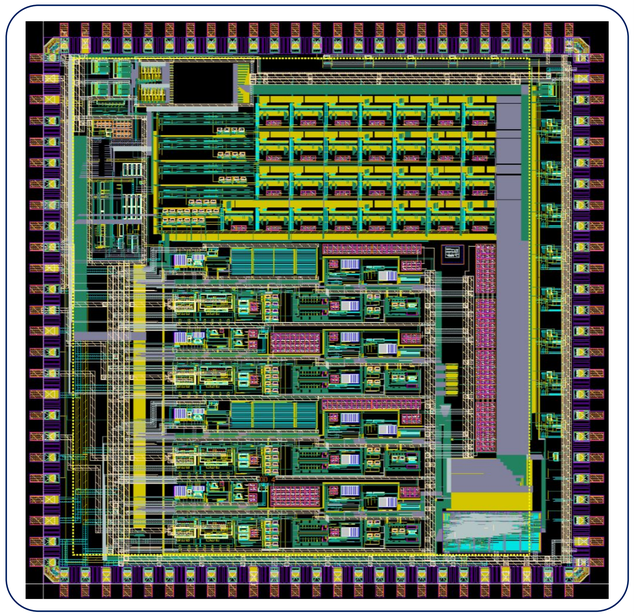
Design of Real-Time Fast Neutron/Gamma PSD

- Each SOUT input signal is split into two fully differential sub-circuits in parallel: one each for total and partial integrations
- A tunable resistor in the total integration circuit is used to set a threshold on the ratio of partial/total integrals
- Figure on the right shows results on neutron/gamma separation using this method, albeit implemented in software. A clear range of threshold space is available for optimizing efficiency vs. leakage
- The PSD threshold can be energy dependent and adjusted to match response of particular scintillators.
- We have implemented fine-tuning of partial (up to 200ns) and total integration lengths (up to 2.5us)
- The tunable resistor value is set by a switchable resistor array, providing 16 resistance settings. This gives a large parameter space in order to be adaptable to various scintillators

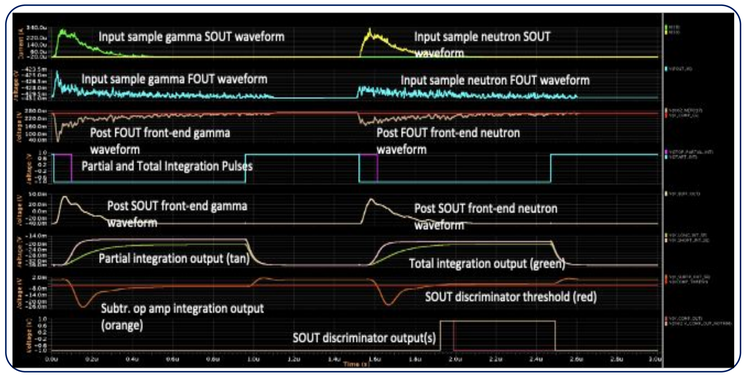


Detailed Overview of PSD_CHIP_v2

- These prototype chips have 100 I/O pads
- Input pads include four SiPM pixels' FOUT, SOUT outputs
- Output pads include buffered, post front-end FOUT, SOUT waveforms; outputs of partial and total integration channels, subtraction op amp, SOUT classification discriminator output for each of four channels and four digital test buses
- The synthesized digital core is responsible for all programmability/tunability selection on-chip
  - 62 on-chip 8-bit registers allow for tuning various baseline reference and comparator threshold voltages, the partial and total integration lengths (including fine-tuning per channel), biases for various circuit blocks, etc
- The chip allows for evaluation of two different designs that implement the programmable digital delay lines necessary for fine tuning of the partial and total integration enable pulses
- The first method involves a chain of (different length) current starved inverters
  - These inverters operate by limiting rise and fall times based on the supplied bias current
  - Bias current is set by a 5-bit current DAC that takes as input the LSB current value
    - This value can be constant or set using an external DAC (it is an input pad to the chip)



A screenshot of the final layout of PSD_CHIP_v2 as taped-out.



Demonstration of the various key signal processing stages of the chip including a final real-time classification of an incident particle as fast neutron vs gamma.

- Can theoretically hit any integration window length up to the max value (fixed by the length of the inverter chain)
  - Step size/resolution set by external DAC specs and noise limitations
- The second method involves a voltage ramp generator setup. A T0 pulse starts the linear charging of a capacitor through a (tunable) constant current source, for the total/partial integration enable pulses. When the capacitor voltage hits a selected threshold, the ramp generator resets and brings the enable pulse LOW again
- The threshold is tunable in 256 linear ~10ns steps for total int and 256 linear ~1ns steps for partial int.

Discussion/Summary

- PSD_CHIP_v2 has been designed, laid out and taped out for fabrication on a 180nm commercial process node.
- A second custom printed circuit board (PCB) has been designed for the initial verification and testing of PSD_CHIP_v2. Boards are currently being fabricated for testing.
  - The board will test/tune all onboard programmability through the custom serial interface line for the chip
  - Initially, an arbitrary waveform generator (AWG) will be used to mimic FOUT and SOUT signal inputs before directly interfacing to a SiPM test bed that will directly couple the outputs from a SensL SiPM to the input of the test board

Links to Program Objectives

- The development of a portable neutron camera is part of the NNSA mission for non-proliferation detection applications.
- Its low power consumption makes it suitable for remote deployment.
- The ASIC that is being developed will find use in NNSA related projects outside of the neutron imaging regime.

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